

N-channel 650 V, 0.058 Ω typ., 48 A MDmesh™ DM2 Power MOSFET in a TO-247 package

Datasheet - production data

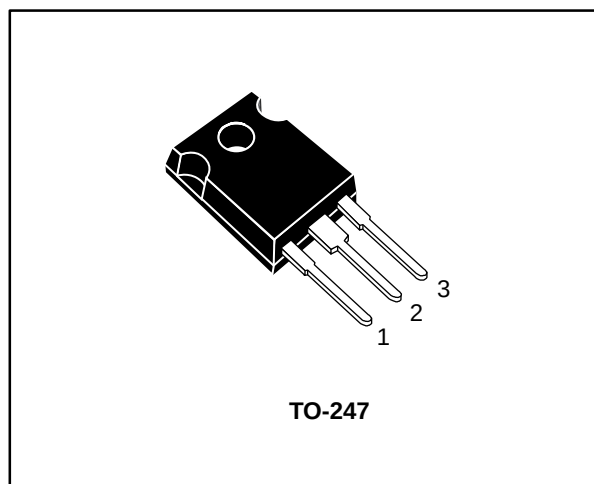
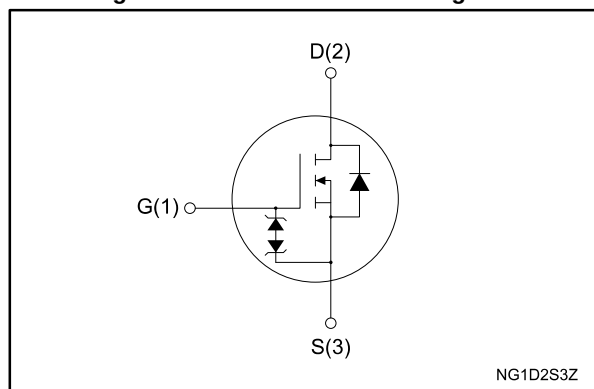


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STW56N65DM2	650 V	0.065 Ω	48 A	360 W

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STW56N65DM2	56N65DM2	TO-247	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	48	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	30	
$I_{DM}^{(1)}$	Drain current (pulsed)	192	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	360	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature		

Notes:

(1) Pulse width is limited by safe operating area.

(2) $I_{SD} \leq 48\text{ A}$, $di/dt = 900\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$

(3) $V_{DS} \leq 520\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.35	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	50	

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive	7	A
$E_{AS}^{(1)}$	Single pulse avalanche energy	1300	mJ

Notes:

(1) starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	650			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 650 V			10	μA
		V _{GS} = 0 V, V _{DS} = 650 V, T _{case} = 125 °C			100	
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±5	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 24 A		0.058	0.065	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	4100	-	pF
C _{oss}	Output capacitance		-	160	-	
C _{rss}	Reverse transfer capacitance		-	2.5	-	
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{DS} = 0 to 520 V, V _{GS} = 0 V	-	375	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	4.1	-	Ω
Q _g	Total gate charge	V _{DD} = 520 V, I _D = 48 A, V _{GS} = 10 V (see Figure 15: "Test circuit for gate charge behavior")	-	88	-	nC
Q _{gs}	Gate-source charge		-	22	-	
Q _{gd}	Gate-drain charge		-	37	-	

Notes:

⁽¹⁾ C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 325 V, I _D = 24 A R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	28	-	ns
t _r	Rise time		-	31	-	
t _{d(off)}	Turn-off delay time		-	157	-	
t _f	Fall time		-	7.7	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		48	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		192	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 48\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 48\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	135		ns
Q_{rr}	Reverse recovery charge		-	0.68		μC
I_{RRM}	Reverse recovery current		-	10		A
t_{rr}	Reverse recovery time	$I_{SD} = 48\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	260		ns
Q_{rr}	Reverse recovery charge		-	2.75		μC
I_{RRM}	Reverse recovery current		-	21		A

Notes:

⁽¹⁾ Pulse width is limited by safe operating area.

⁽²⁾ Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

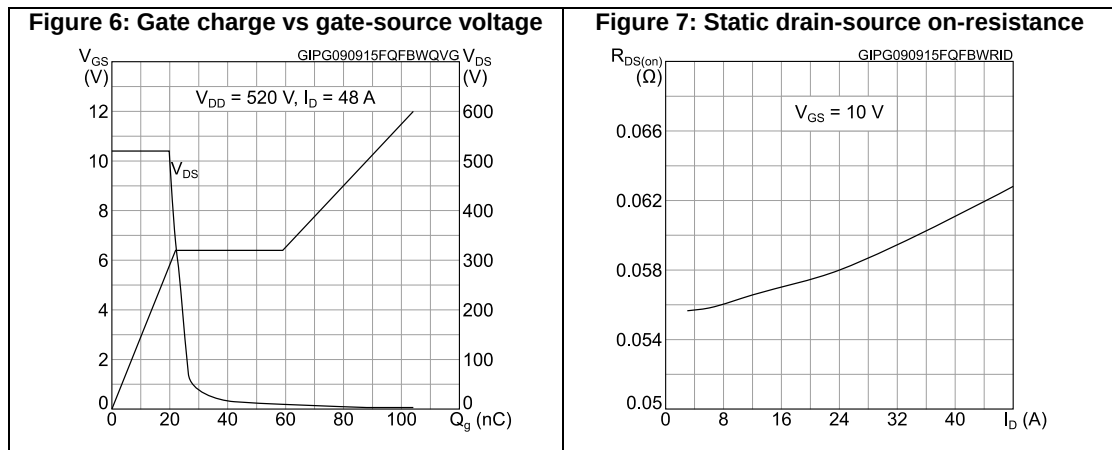
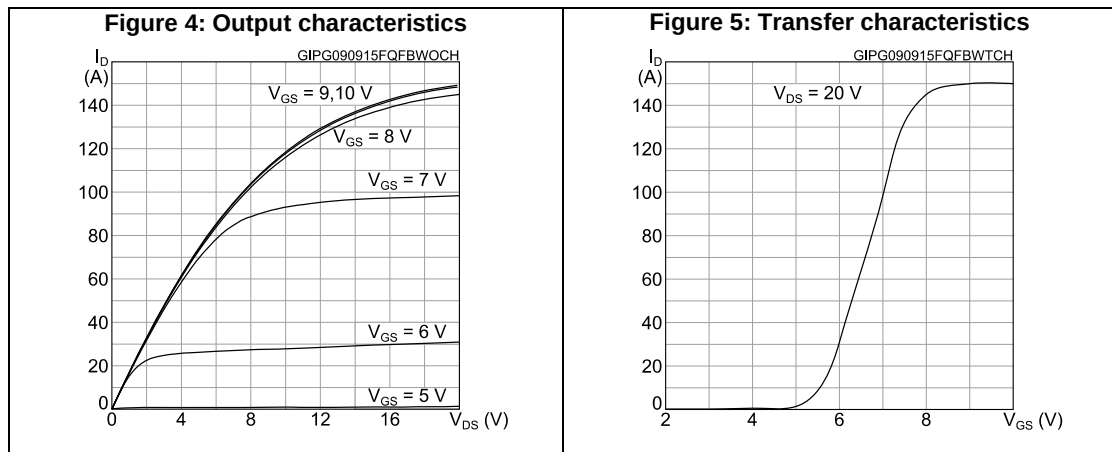
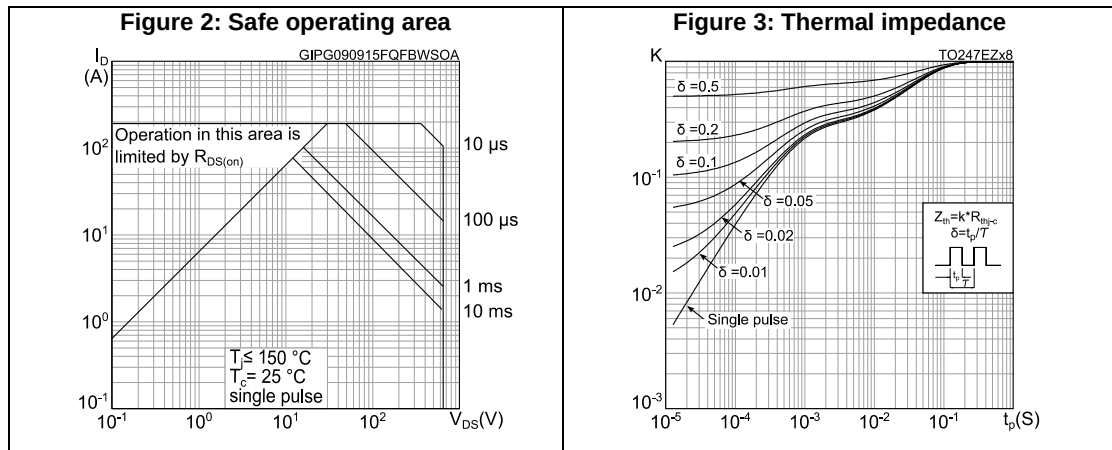


Figure 8: Capacitance variations

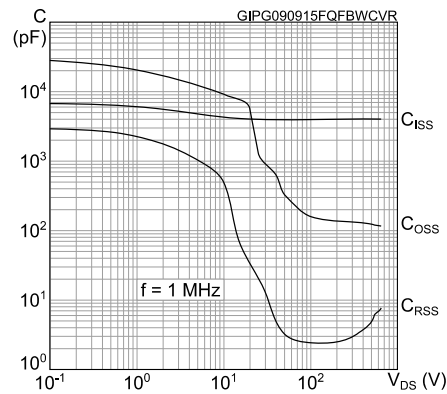


Figure 9: Normalized gate threshold voltage vs temperature

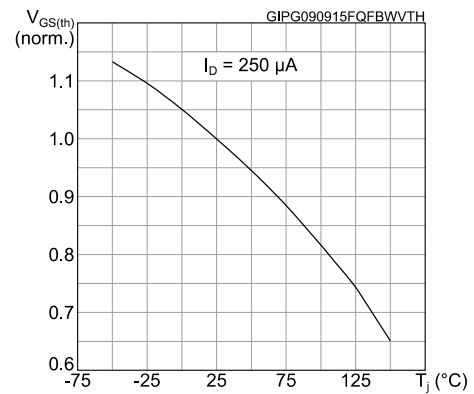


Figure 10: Normalized on-resistance vs temperature

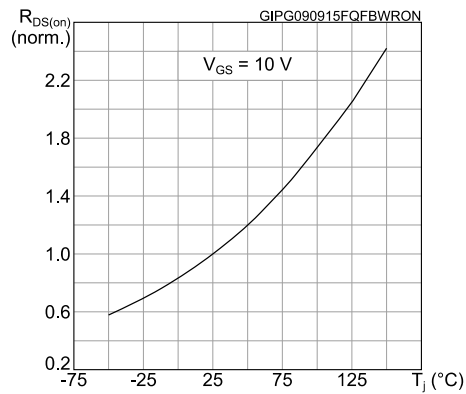


Figure 11: Normalized V(BR)DSS vs temperature

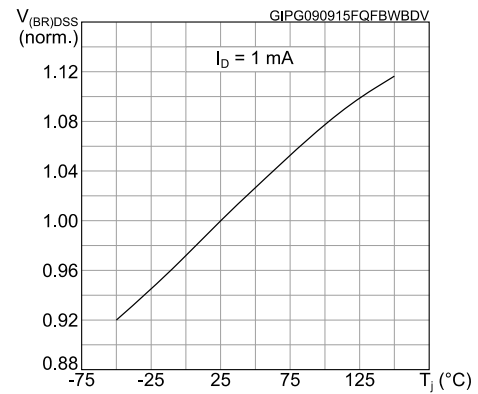


Figure 12: Output capacitance stored energy

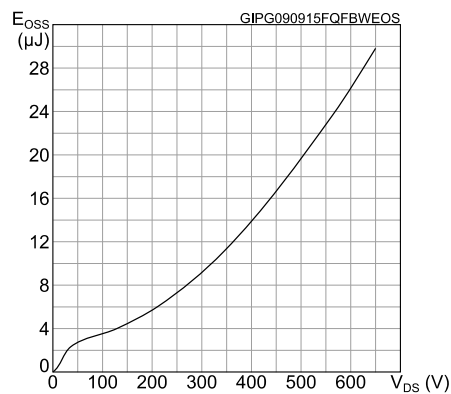
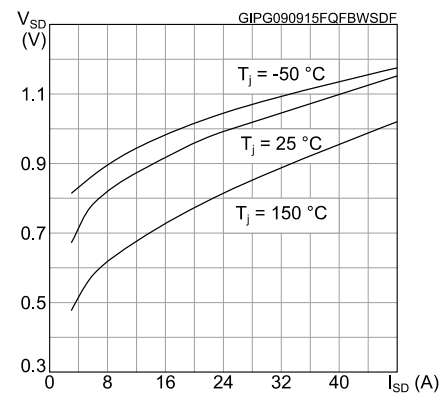


Figure 13: Source- drain diode forward characteristics



3 Test circuits

Figure 14: Test circuit for resistive load switching times

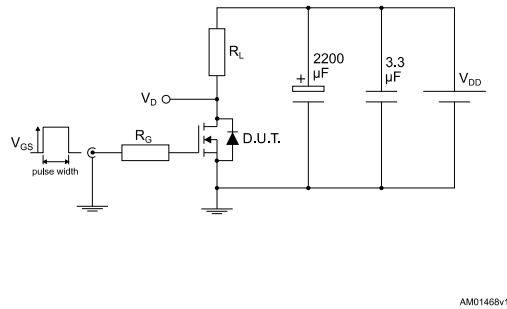


Figure 15: Test circuit for gate charge behavior

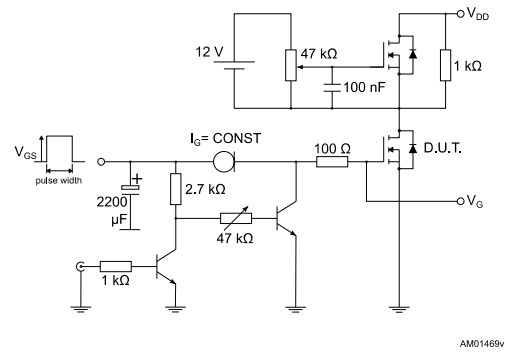


Figure 16: Test circuit for inductive load switching and diode recovery times

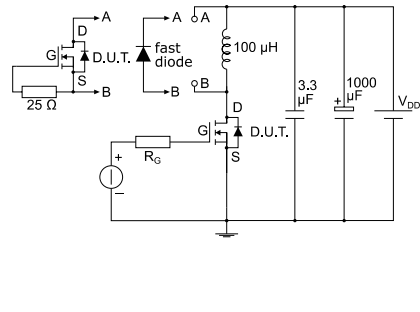


Figure 17: Unclamped inductive load test circuit

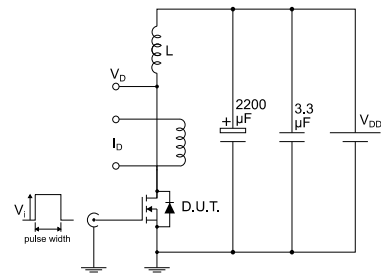


Figure 18: Unclamped inductive waveform

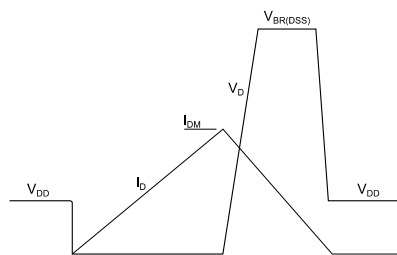
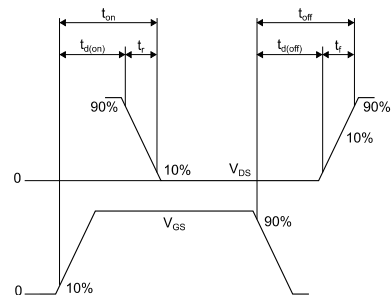


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 20: TO-247 package outline

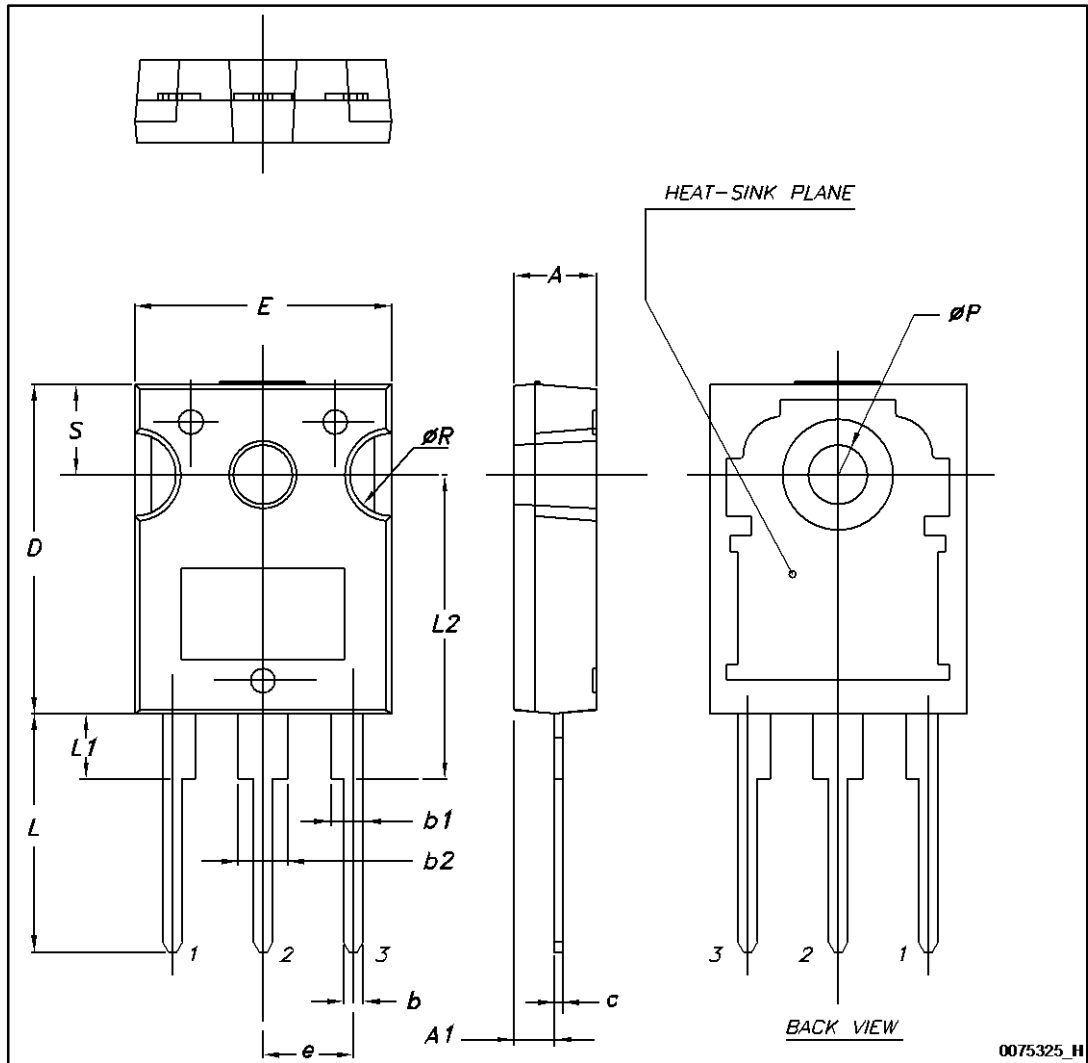


Table 9: TO-247 package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
27-Nov-2014	1	First release.
15-Sep-2015	2	Text and formatting changes throughout document. In section <i>Electrical ratings</i> : - updated tables <i>Absolute maximum ratings</i> and <i>Avalanche characteristics</i> In section <i>Electrical characteristics</i> : - updated and renamed table <i>Static</i> (was On/off states) - updated tables <i>Dynamic</i> , <i>Switching times</i> and <i>Source-drain diode</i> Updated section <i>Electrical characteristics (curves)</i>

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